7. The interpolation circuit according to claim 2, characterized by comprising data appending unit for appending data having the symmetrical values proportional to the input data before and after said input data in the former stage of said oversampling operation unit.

8. The interpolation circuit according to claim 3, characterized by comprising data appending unit for appending data having the symmetrical values proportional to the input data before and after said input data in the former stage of said oversampling operation unit.

9. The interpolation circuit according to claim 4, characterized by comprising data appending unit for appending data having the symmetrical values proportional to the input data before and after said input data in the former stage of said oversampling operation unit.

10. The interpolation circuit according to claim 5, characterized by comprising data appending unit for appending data having the symmetrical values proportional to the input data before and after said input data in the former stage of said oversampling operation unit.

In the Drawings:

Please amend FIG. 19 as indicated in red on the drawing sheet attached herewith.